ABSTRACT

Buffering data transfer between a chipset and memory modules is disclosed. The disclosure includes providing and configuring at least one buffer. The buffers are provided in an interface between a chipset and memory modules. The buffers allow the interface to be split into first and second sub-interfaces. The first sub-interface is between the chipset and the at least one buffer. The second sub-interface is between the at least one buffer and the memory modules. The buffers are then configured to properly latch the data being transferred between the chipset and the memory modules. The first and second sub-interfaces operate independently but in synchronization with each other.